REMARKS

Claims 1, 2, 4-14, and 16-23 are pending. Claims 1, 4, 7, 9, and 16-19 have been amended, and claims 3 and 15 have been canceled.

Reconsideration of the application is respectfully requested for the following reasons.

In the Office Action, the Examiner rejected claims 1-3, 5, 6, 8-11, and 20-23 under 35 U.S.C. §102(e) for being anticipated by the Arimilli publication. This rejection is traversed for the following reasons.

Claim 1 recites broadly embodiments of the invention disclosed in the specification. In particular, claim 1 has been amended to recite that the "bus snooper performs the update algorithm by operating a placement algorithm using cache block information from a prescribed logic operation which includes a divide and conquer tree." These features are taken from allowable claims 4 and 7. Accordingly, it is submitted that claim 1 is allowable in its amended form along with all claims depending therefrom.

Claim 9 has been amended to recite the features of allowable claim 15, which has been canceled from the application. Accordingly, it is submitted that claim 15 and its dependent claims are in allowable form.

Claim 21 recites a multiprocessor system comprising a plurality of processors coupled to a processor bus, and at least one cache memory coupled to each processor. In addition to these features, claims 21 recites a "cache flush system coupled to the processor bus."

The cache flush system includes a first unit configured to "provide cache status information for the at least one cache memory coupled to each of the processors," a second

unit configured to "update the cache status information for the at least one cache memory coupled to each of the processors," and a third unit configured to "detect system events to perform cache flushing for corresponding cache blocks and the at least one cache memory coupled to each of the processor in a prescribed state responsive to the detected event." The Arimilli publication does not disclose the cache flush system of claim 21.

The Arimilli publication discloses a system for managing a plurality of processors coupled to a interconnect link 58. Each processor includes a CPU 54 and a corresponding cache memory 62. See Figures 2A and 2B. Each of the processors further includes a memory controller MC which perform a variety of operations, including detecting status information of their respective cache memories. This includes memory coherency operations performed according to an MESI protocol. See, for example, paragraph [0050]. Each of the memory controllers also performs cache flush and write-back operations.

However, unlike claim 21, the Arimilli system does not include a cache flush system which manages cache flush operations for a plurality of cache memories coupled to a respective plurality of processors. On the contrary, the cache flush operations are separately performed by the memory controllers coupled to each individual processor (CPU) of the Arimilli system. See Figures 2A and 2B. Thus, the Arimilli publication does not disclose or suggest the use of a cache flush system to control a cache flush operations for a plurality of caches, each coupled to a respective one of a plurality of processors as recited in claim 21.

Absent these features, it is clear that the Arimilli publication does not disclose the first unit, the second unit, and the third unit recited in claim 21. To make these differences

more evident, claim 21 has been amended to recite that these units perform their respective operations for or in "the at least one cache memory coupled to each of the processors." More specifically, the first unit provides "cache status information for the at least one cache memory coupled to each of the processors." The Arimilli publication does not disclose these features.

The second unit updates "the cache status information for the at least one cache memory coupled to each of the processors." The Arimilli publication does not disclose these features.

The third unit detects "system events to perform cache flushing for corresponding cache blocks in the at least one cache memory coupled to each of the processors in a prescribed state responsive to the detected event." The Arimilli publication does not disclose these features.

Because the Arimilli publication does not disclose all the features recited in claim 21, it is respectfully submitted that the Arimilli publication cannot anticipate this claim. Applicants further submit that these differences are sufficient to render claim 21 and its dependent claims non-obvious and thus patentable over the Arimilli publication.

Claim 22 recites that the second unit is configured to "update the cache status information by monitoring the processor bus and by tracing a state of each cache memory." The Arimilli publication does not disclose these features. As shown in Figures 2A and 2B, the memory controller coupled to each processor controls a flushing operation for an associated cache memory. The Arimilli publication does not disclose a single cache flush

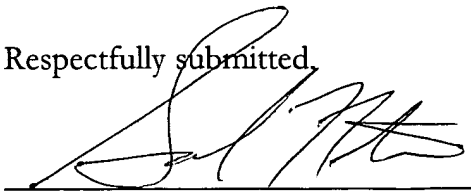
system for managing the caches coupled to a plurality of processors, "by tracing a state of each cache memory" as recited in claim 22. Applicants respectfully submit that claim 22 is allowable for these additional reasons.

Claim 23 recites a valid array unit which provides cache block information for an update algorithm and index information for a cache flush algorithm "of at least one cache block and the at least one cache memory coupled to each of the processors in a prescribed state." The Arimilli publication does not disclose these features.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of the application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with this application to Deposit Account No. 16-0607 and credit any excess fees to the same Deposit Account.

Respectfully submitted,



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